Amendments to the Specification

1. Please amend the title of the application as follows:

HYBRID ELECTRICAL CIRCUIT METHOD ~~DEVICE~~ WITH MATED SUBSTRATE CARRIER METHOD

2. Please replace the first five consecutive paragraphs of the "BACKGROUND OF THE INVENTION" section of the application, commencing at page 1, line 5 of the application, with the following amended paragraphs:

In the development of radio frequency circuits and especially microwave radio frequency circuits two different approaches to experimental or work in progress circuit implementation are often used. These approaches are the monolithic microwave integrated circuit (MMIC) and the hybrid integrated circuit. The MMIC process consists here of an entire circuit including active and passive elements being fabricated on a part of a wafer of semiconductor material. In the hybrid approach, the active element(s) is/are fabricated on a semiconductor material wafer and the remaining portions of the circuit are fabricated on a dielectric substrate. The individual parts are then assembled on a solid metal carrier that holds the circuit together mechanically. The carrier also provides a common ground plane and acts as a thermal heat sink.

The MMIC has the advantage of being very small, accurate, and repeatable and is indeed the ultimate goal of many circuit development efforts. Some disadvantages of the MMIC technique are however the large investment in time and other resources needed for each new iteration of a design, the imposed small circuit size (which limits the electrical size of the passive elements and types of circuit elements that are realizable), a minimum tuning capability, and a wasting of active semiconductor material to make passive components. The hybrid circuit offers advantages with respect to design flexibility as a result of its larger size, increased range of tuning to meet ~~the~~ specifications, and the avoidance of costly device material waste on passive component realization. Hybrid circuits suffer from being considerably larger in physical size, and more importantly have limited accuracy and repeatability characteristics. These inaccuracies stem from an assembly process not having the tight tolerances of semiconductor fabrication technology. Notwithstanding these difficulties however the hybrid integrated circuit remains a necessary part of the development cycle for many circuits and indeed the final configuration of many ~~integrated~~ circuit designs particularly in the radio frequency and microwave integrated circuit arts.

It is perhaps worth mention in this background discussion that a radio frequency signal processing circuit and particularly a transmitter circuit intended for use in the microwave range of radio frequencies is, in one of its most technically challenging portions, (i.e., the signal output stage) a power handling circuit, i.e., a circuit capable of generating a specified number of watts of output signal power from a lesser number of watts of input signal power while functioning at an elevated

operating frequency. The need for significant output power levels and the absence of high power handling efficiency in such circuits, especially when some form of linear or "class A" circuit operation rather than the more energy efficient "class C" operation is dictated, results in a need for such circuits to have significant power dissipating capability, dissipation without exceeding the operating temperatures acceptable for semiconductor device operation. This power dissipating need usually precludes the mounting of a radio frequency circuit die directly on a ceramic substrate member in a hybrid integrated circuit arrangement for example and requires that an efficient and direct thermal energy circuit be established between the dissipating semiconductor device and some metallic heat sink such as the substrate carrier of the present invention. It is this needed heat dissipating capability which dictates disposition of the radio frequency circuit die in the present invention within an aperture of the substrate member and into direct metallic connection with a chip carrier recess-received pedestal member. In this disposition of the radio frequency circuit die, bond wires may be used to advantage in making connections between the substrate conductor nodes and the circuit die connection pads.

Considering now a related but somewhat different aspect of a hybrid integrated circuit device, circuit designers typically attempt to minimize the length of the bond wires used within an integrated circuit package to for example connect a circuit die to external package pins. This minimizing limits a frequent source of circuit variability and is usually accomplished through use of one or more of three techniques. A first of these techniques involves use of a very thin dielectric material substrate to fabricate the circuit pattern. A typical active device measures four mils in thickness for example and the dielectric materials typically range from 8 mils to 30 mils in thickness for microwave operation. If the designer uses a thin dielectric material (of say 10 mils thickness), the active device can be mounted on a flat carrier and the bond wires will stretch 6 mils from the top of the active device up to the surface of the dielectric material. This arrangement is shown in FIG. 26A and FIG. 26B of the drawings herein where cross sectional and top views appear. FIG. 26A is enlarged and FIG. 26B is of approximately real device size in these drawings. The layer of for example tin/lead solder used to attach the substrate to the substrate carrier in the FIG. 26A drawing and also in the present invention hybrid devices is identified at 2600 in FIG. 26.

In the FIG. 26A and FIG. 26 B drawings the carrier is simple to design and fabricate. However, the thinner dielectric material in the substrate limits the networks a designer can realize on the dielectric material surface. With such thin dielectric material for example the fabrication rules usually impose a fixed minimum line width. Thinner dielectric materials in a substrate require smaller line widths to get the same characteristic impedance as is usually achieved with thicker dielectrics. Thus, a thinner dielectric will not realize the high impedance characteristics of a thicker dielectric material.

3. Please replace the three consecutive paragraphs commencing at page 6, line1 in the application with the following amended paragraphs:

The accompanying drawings incorporated in and forming a part of the specification, ~~illustrates~~ illustrate several aspects of the present invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1A represents ~~shows~~ a top view of a milling machine usable in fabricating a substrate carrier according to the present invention.

FIG. 1B represents ~~shows~~ a front, motor-up, view of a milling machine usable in fabricating a substrate carrier according to the present invention.

4. Please replace the paragraph commencing at page 9, line 21 in the application with the following amended paragraph:

The Compact Disc appendix included in the U.S. Patent and Trademark Office file of the present patent document ~~has been prepared in response to the PTO procedure effective March 1, 2001 for submission of 37 C.F.R. 1.96(c) computer code listings. This disc has been~~ is submitted in the form of two identical disc copies each including two file folders ~~of computer files; i.e., computer code files~~. One of these file folders, the folder "uccas_code" is of 99.1 Kilobytes (101,559 bytes) size, contains 42 individual files and is dated September 24, 2001; this file folder ~~and included files~~ discloses software code used in embodiment of the invention. The second of these file folders, the folder "uccas_examples" is of 898 bytes size, contains 3 individual files and is dated September 24, 2001; this file folder discloses sample data usable to verify operation of the invention. The contents of these compact disc file folder materials are hereby incorporated by reference herein.

5. Please replace the paragraph commencing at page 45, line 15 in the application with the following amended paragraph:

FIG. 29 in the drawings shows an exploded perspective view of a 15-via hybrid device made in accordance with the present invention. The FIG. 29 device includes a substrate carrier 2900, a substrate 2902 and an array 2904 of network elements embodied in the form of shaped conductors located on the substrate 2902 surface. FIG. 29 also shows the mating recess 2906 in the substrate carrier 2900 and a plurality of recess-received pillars such as the pillar 2908. Notably the hole 2910 in the substrate 2902 is reserved for substrate topside component use and does not have a mating pillar in the recess 2906. A representative dimension for the substrate 2902, expressed in fractional inch units, appears at 2912 in FIG. 29; smaller or larger substrates are of course possible within the scope of the invention. A representative arrow indicating the exploded nature of the FIG. 29 view and the intended final disposition of the substrate 2902 appears at 2914 in the FIG. 29 drawing. The

substrate 2902 may be made of a machineable radio frequency dielectric material such as one of the materials available from Rogers Corporation of One Technology Drive, PO Box 188, Rogers Ct., 06263-0188; http://www.rogers-corp.com/ ~~WWW. Rogers-Corp.Com~~.

6. Please replace the "ABSTRACT" on page 52 of the application with the following amended paragraph:

A hybrid integrated circuit fabrication method ~~arrangement~~ in which an insulating substrate member and its metallic substrate carrier are made to be mating ~~mated~~ with precision through use of computer controlled machining performed on each member. A combination of disclosed specifically tailored software and commercially available software are used in the method to generate code for controlling ~~used to control~~ a precision milling machine during the fabrication of substrate and substrate carrier members. The method for precision mating of substrate and substrate carrier enable disposition of a precision recess in the substrate carrier and the location of recess pillars and pedestals (the latter being for integrated circuit die mounting use) at any carrier recess location desirable for electrical, thermal or physical strength reasons. Enhanced electrical thermal and physical properties are achieved in hybrid devices fabricated according to the method ~~invention~~ especially when compared with devices and methods having the limited availability of comparable elements afforded by previous hybrid fabrication arrangements.